

JEDEC STANDARD

DDR_x Spread Spectrum Clocking (SSC) Standard

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR_x SPREAD SPECTRUM CLOCKING (SSC)

(From JEDEC Board Ballot JCB-20-13, formulated under the cognizance of the JC-42.3C Subcommittee on DRAM Parametrics.)

1 Scope

Definition for all DDR_x component documents to reference. This is generic to any DDR_x technology.

2 Terms and definitions

$f_{CK,min}$: Minimum frequency supported by the DRAM (for all speed bins, $1/t_{CK(avg),max}$)

$f_{CK,max}$: Maximum frequency supported by the DRAM ($1/t_{CK(avg),min}$)

$f_{SSC,nom}$: Mean frequency of $f_{SSC,min}$ and $f_{SSC,max}$

SSC band: If the system modulates the input clock frequency between $f_{SSC,min}$ and $f_{SSC,max}$, this frequency band is referred to as the SSC band

Modulation frequency: Rate at which the frequency is modulated for SSC

example: 20 kHz modulation: Input clock frequency shifts gradually from $f_{SSC,min}$ to $f_{SSC,max}$ over 25 us (=50 us/2)

3 SSC Criteria

SSC is allowed only if $f_{SSC,min}$ is greater than or equal to $f_{CK,min}$ and $f_{SSC,max}$ is less than or equal to $f_{CK,max}$. All input clock specs including, but not limited to, $t_{err(nper)}$ must be met at all times. Allowed modulation frequency is 20 kHz to 60 kHz.

4 Allowed SSC band

If the DRAM DLL is locked at $f_{SSC,nom}$ (by issuing a DLL reset and waiting t_{DLLk}) and then the SSC is later turned on, the system is allowed an SSC band of $f_{SSC,nom} \pm 1\%$.

In all other cases, the system is allowed an SSC band of $f_{SSC,nom} \pm 0.5\%$.

If the input clock frequency drifts out of this band, the output timings can no longer be guaranteed and DLL reset must be issued to regain the output timings assuming a different SSC band.



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☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

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